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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,112	06/24/2003	Richard K. Williams	ATI002US	3705

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PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/606,112	WILLIAMS ET AL.
	Examiner	Art Unit
	Matthew E. Warren	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6 and 10-17* is/are rejected.

7)☒ Claim(s) *2,5,7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election and Amendment filed on January 10, 2005.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are informal and are so poor in quality that it is difficult to determine all of the elements of the invention. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

Claim 1 is objected to because of the following informalities: in line 14 of the claim, the limitation of "gate control a..." should be "gate controls a...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 6, 10, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Hshieh (US 6,262,453 B1).

In re claim 1, Hshieh shows (fig. 4) a semiconductor device comprising: a substrate (105) of a first conductivity type (N); a gate structure (125) in a plurality of trenches in the substrate, wherein in each of the trenches, the gate structure comprises a conductive gate surrounded by an insulating material (120) that has a first thickness at a sidewall of the trench and a second thickness (120') at a bottom of the trench, the second thickness being greater than the first thickness; a first region (138) of a second conductivity type (P) adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including channel region adjacent to the trenches; a second region (130) of the second conductivity type, wherein the second region is in electrical contact with the first region, and the second regions extends to a second depth that is deeper than the first depth and shallower than the trenches; and a third region (140) of the first conductivity type atop the first region, wherein a voltage on the conductive gate control a current flow from the third region through the first region to an underlying portion of the substrate.

In re claim 3, Hshieh shows (fig. 4) that the substrate comprises a first semiconductor layer (110) atop a semiconductor substrate that is more heavily doped

(N+) than the first semiconductor layer, wherein the trenches extend into the first semiconductor layer.

In re claim 6, Hshieh discloses (col. 7, liens 47-62) that the voltage on the conductive gate controls a current flow from the third region through first region and through the first semiconductor layer to the semiconductor substrate.

In re claim 10, Hshieh shows (fig. 4) that the first region and the third region are in a first mesa between a first pair of the trenches (two trenches shown); and the second region is between a second pair of the trenches (between the right most trench shown and an additional adjacent trench not shown).

In re claim 17, Hshieh shows (fig. 4) that the second region (130) has a concentration (p) of dopants of the second conductivity type that is higher than that (p-) of the first region (138).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (US 6,262,453 B1) as applied to claim 1 above, and further in view of Funaki et al. (US 6,211,549).

In re claim 4, Hshieh shows (fig. 3J) that the substrate further comprises a second semiconductor layer (130) atop the first semiconductor layer, but does not disclose that the second semiconductor layer is more lightly doped than the first semiconductor layer. Funaki et al. shows (fig. 2) that a second semiconductor layer (21) is formed atop a first semiconductor layer (22), and that the second semiconductor layer is more lightly doped than the first semiconductor layer. With this configuration a device having a high breakdown voltage is formed (col. 6, lines 6-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second semiconductor layer of Hshieh by doping that layer more lightly than a first semiconductor layer as taught by Funaki to form a device having a high breakdown voltage.

Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (US 6,262,453 B1) as applied to claim 1 above, and further in view of the Applicant's Prior Art Figure 3A (APAF).

In re claim 11, Hshieh shows all of the elements of the claims except the device further comprising a fourth region of the second conductivity type, wherein the fourth region is at a surface of the substrate and extends across an entire separation between the second pair of trenches. The APAF 3A shows an additional region (206D) as a fourth region at a surface of the substrate and extending across an entire separation between the second pair of trenches (205C and 205D). By forming this region between a second pair of trenches, a protective diode-only cell can be formed to provide

additional protection to the device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trenched gate device of Hshieh by forming a fourth region at the substrate surface between a second pair of trenches as taught by the APAF to form a protective diode-only cell for device ESD protection.

In re claim 14, the APAF 3A shows that the second region (209) extends to a first plurality of adjacent mesas that are between pairs of the trenches (205C and 205D) and is absent from a second plurality of adjacent mesas that are between pairs of the trenches (205B and 205C).

Claims 12 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (US 6,262,453 B1) as applied to claim 1 above, and further in view of Hshieh et al. (US 5,689,128).

In re claim 12, Hshieh ('453) shows (fig. 4) a mesa between a first and a second of the trenches comprises: the third region (140) at a surface of the substrate and adjacent to the first trench; a fourth region of the first conductivity type at the surface of the substrate and adjacent to the second trench (140 left side of second rightmost trench); a fifth region (160) of the second conductivity type between the third and fourth regions at the surface of the substrate; the first region (138) underlying the third and fourth regions. Hshieh shows all of the elements of the claim except the second region underlying the third region and separated from the first and second trenches. Hshieh ('128) shows (fig. 2) a semiconductor device having a second region (36) underlying the

third region (20) and separated from first and second trenches (24) to reduce the occurrence of a parasitic JFET (col. 4, lines 7-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second region of Hshieh ('453) by forming that second region separate from the first and second trenches as taught by Hshieh ('128) to eliminate parasitic JFET action.

In re claim 13, Hshieh ('453) shows (fig. 4) an electrical contact (170) to the third, fourth, and fifth regions.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh (US 6,262,453 B1) as applied to claim 1 above, and further in view of Calafut et al. (US 6,396,102).

In re claims 15 and 16, Hshieh shows all of the elements of the claims but does not specifically show the device further comprising a gate bus that is electrically connected to the gate structure in the trenches, wherein the gate bus overlies a portion of the substrate that includes at least part of the first region or the second region. Calafut et al. shows (fig. 4F) a trenched MOSFET having a bus surface structures 46a, 46b, 46c) over the trenches and connected to the gates within the trench. These surface structures provide a voltage to the gates within the trenches. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trenched gates of Hshieh by connecting a gate bus structure to the trenched gates and over the regions of the substrate as taught by Calafut to provide a voltage to the gates in the trenches.

Allowable Subject Matter

Claims 2, 5, and 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
April 1, 2005

GEORGE ECKERT
PRIMARY EXAMINER